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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 10/010,161 | 11/13/2001 | Brian C. Barnes | 2000.056700 | 7264 |

23720- 7590 06/29/2006

WILLIAMS, MORGAN & AMERSON
10333 RICHMOND, SUITE 1100
HOUSTON, TX 77042

| EXAMINER | |
|---|---|
| ABYANEH, ALI S | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2137 | |

DATE MAILED: 06/29/2006

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**BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES**

Application Number: 10/010,161
Filing Date: November 13, 2001
Appellant(s): BARNES ET AL.

Sanjeev K. Singh

For Appellant

**EXAMINER'S ANSWER**

This is in response to the appeal brief filed 04-17-2006 appealing from the Office action mailed 11-15-2005.

**(1) Real Party in Interest**

A statement identifying by name the real party in interest is contained in the brief

**(2) Related Appeals and Interferences**

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

**(3) Status of Claims**

The statement of the status of claims contained in the brief is incorrect. A correct statement of the status of the claims is as follows:

Claims 1-9, 11-19, 21, 23-25, 27-34, 36 and 37 were rejected under 35 U.S.C. 102(b) by Maruyama et al. (US Patent NO 6,052,763).

Claims 10, 20, 22, 26 and 35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Maruyama (6,052,763) in view of applicant's admitted prior art.

**(4) Status of Amendments After Final**

No amendment after final has been filed.

**(5) Summary of Claimed Subject Matter**

The summary of claimed subject matter contained in the brief is correct.

**(6) Grounds of Rejection to be Reviewed on Appeal**

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

**(7) Claims Appendix**

The copy of the appealed claims contained in the Appendix to the brief is correct.

**(8) Evidence Relied Upon**

6052763 Maruyama 4-2000

Applicants admitted prior art (Specification, Description of the related art, page 5, lines 4-18)

**(9) Grounds of Rejection**

The following ground(s) of rejection are applicable to the appealed claims:

**Claim Rejections - 35 USC § 102**

Claims 1-9,11-19, 21, 23-25, 27-34, 36 and 37 are rejected under 35 U.S.C. 102(b) as being anticipated by Teruyuki Maruyama et al. (US Patent NO.6,052,763).

**Regarding Claims 1, 11-13, 23, 32 and 36-37**

Maruyama teaches a processing unit 340 (execution unit) coupled to the memory unit 10 through the use of bus 15 and a memory controller 20 (memory management unit) coupled to the DRAM memory 19 (column 4, lines 62-67, column 6, lines 1-19 and fig 4). Maruyama furthermore teaches a memory management unit for managing a memory storing data arranged within a plurality of memory pages, the memory management unit comprising: a security check unit (register 21) coupled to receive a linear address generated during execution of a current instruction (column 5, line 20-21), wherein the linear address has a corresponding physical address residing within a selected memory page [(column 5, line 23-24) (access address is accessing a range within DRAM 19. DRAM 19 has to be addressed by physical address)], and wherein the security

check unit is configured to use the linear address to access at least one security attribute (processor master ID) data structure located in the memory to obtain a security attribute of the selected memory page, to compare a numerical value conveyed by a security attribute of the current instruction to a numerical value conveyed by the security attribute of the selected memory page, and to produce an output signal dependent upon a result of the comparison, if the processor master ID does not match, the comparator outputs a signal indicating an error (fault signal); if there is a match a different signal is outputted [(access addresses are stored in the decoder and master ID is sent to register 22. A comparator 23 is used to compare the master ID from the system bus with the bus master ID and outputs a signal)(column 6, lines 11-40 and column 5 lines 20-40)]; and wherein the memory management unit is configured to access the selected memory page dependent upon the output signal (column 6 lines 29-40). (Having a paging unit is inherent in the art in order to translate linear addresses to physical addresses).

**Regarding Claims 2, 14, 21, 24 and 29**

Maruyama teaches all limitation of the claim as applied to claim 1, 13 and 23 above and furthermore he teaches a master ID data structure 24 comprising a master ID table (table directory) and a lookup table (security attribute table) (column 6, lines 48-54).

**Regarding Claims 3, 15 and 30**

Maruyama teaches all limitation of the claim as applied to claim 2, 14 and 29 above and furthermore he teaches a memory controller 20 (memory management unit), wherein the master ID table (security attribute table directory) comprises a plurality of entries, and where each entry of the security attribute table directory includes a present bit and a security attribute table base address field, and wherein the present bit indicates whether or not a security attribute table corresponding to the security attribute table directory entry is present in the memory, and wherein the security attribute table base address field is reserved for a base address of the security attribute table corresponding to the security attribute table directory entry (column 6, lines 30-55 and fig 4).

**Regarding Claims 4-6, 16-18, 27, 28 and 31**

Maruyama teaches all limitation of the claim as applied to claims 2, 1, 14, 13, 23 and 29 above and furthermore he teaches using a master ID table (accessing one security attribute data structure) to extract a master ID (obtain additional security attribute, SCID) and compare it to master ID of the accessing processor. The master IDs are indicators of security level of accessing processor since they determine if the processor is authorized to perform any transactions in the memory system (column 6, lines 30-55 and fig 4).

**Regarding Claim 7**

Maruyama teaches all limitation of the claim as applied to claims 1, above and furthermore he teaches a memory management unit, wherein the comparator (security check logic) is configured to obtain the master ID (security attribute) of the current instruction from the at least one master ID table (security attribute data structure) (column 6, lines 29-40 and fig 4).

**Regarding Claim 8**

Maruyama teaches all limitation of the claim as applied to claims 1, above and furthermore he teaches a memory management unit, wherein the output signal is a fault signal [(column 6, lines 35-40) (if the processor master ID does not match, the comparator outputs a signal indicating an error (fault signal); if there is a match a different signal is outputted)].

**Regarding Claim 9**

Maruyama teaches all limitation of the claim as applied to claims 1, above and furthermore he teaches a memory management unit, wherein the register 21 (security check unit) is configured to receive a set of processor master ID (security attributes) of the selected memory page in addition to the master ID (security attribute) of selected memory page, and to produce the output signal dependent upon: (i) the result of the comparison of the numerical value conveyed by the master ID (security attribute) of the current instruction to the numerical value conveyed by the master ID (security attribute) of selected memory page,

and (ii) the set of master ID (security attributes) of the selected memory page (column 6, lines 11-40).

**Regarding Claims 19, 25 and 33**

Maruyama teaches all limitation of the claim as applied to claims 13, 23 and 32 above and furthermore he teaches a memory controller 20 (memory management unit), wherein the register unit 21 (security check unit) is coupled to receive a current privilege level (CPL) of a current task including the current instruction, and configured to produce the output signal dependent upon: (i) the result of the comparison of the numerical values conveyed by the security attribute of the current instruction and the security attribute of selected memory page, and (ii) the CPL of the current task including the current instruction (column 6, lines 11-40 and fig 4).

**Regarding Claim 34**

Maruyama teaches all limitation of the claim as applied to claim 32 above and furthermore he teaches using an access address to obtain the master ID (security attribute) for an accessing processor wherein a master ID data structure 24 comprises a master ID table (table directory) and a lookup table (security attribute table) (column 6,lines 48-54).

***Claim Rejections - 35 USC § 103***

Claims 10, 20, 22, 26, and 35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Maruyama (6,052,763) in view of applicant's admitted prior art.

**Regarding Claims 10, 22, 26 and 35**

Maruyama teaches the memory management system of claims 1, 13, and 23. Maruyama does not teach security attributes comprising a user/supervisor (U/S) bit and a read/write (R/W) bit. Applicant's admitted prior art discloses the memory protection features of an user/supervisor (U/S) bit and a read/write (R/W) bit where U/S=0 indicates that the memory page is an operating system page, U/S=1 indicates that the memory page is an user memory page, R/W=0 indicates that only read accesses are allowed, and R/W=1 indicates that both read and write accesses are allowed to the memory page (Page 5, lines 4-18). Therefor It would have been obvious to one of ordinary skill in the art at the time the invention was made to integrate the protection features disclosed in applicant's admitted prior art to the memory management system of Maruyama. This would have been obvious because person having ordinary skill in the art at the time the invention was made would have been motivated to do so since these features would add further security to the system by allowing the further access controls such as user or supervisor assigned memory areas and memory areas assigned as read-only or read-write areas.

**Regarding Claim 20**

Maruyama teaches the memory management system of claim 13. Maruyama does not teach a physical address within a selected memory page including a base address and an offset. Applicant's admitted prior art teaches a lower portion of an address (offset) being used as an index of the memory page and a page frame base address being used to select the corresponding memory page. When the offset and the base address are combined, they form a physical address (Page 4, lines 21-25). Therefore It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Maruyama's system to include a physical address within a selected memory page including a base address and an offset. This would have been obvious because person having ordinary skill in the art at the time the invention was made would have been motivated to do so in order to give the system the ability to produce a physical address from the input of a linear address since such ability would allow the system in the case where linear addresses are being inputted.

**(10) Response to Argument**

Applicant's argument that "Maruyama does not teach, disclose or suggest using a linear address to access at least one security attribute data structure located in a memory to obtain a security attribute of a selected memory page in the memory" is not persuasive because Maruyama teaches a processor 340 is connected through a bus 15 to a memory unit 10, the memory unit 10 includes a DRAM 19 and a Master ID Table 24 (see column 5, lines 7-11). Maruyama also discloses using a linear address and

accessing at least one security attribute data structure (Master ID Table 24) located in a memory (memory unit 10) to obtain a security attribute of a selected memory page in the memory (see column 5, lines 20-40).

Applicant's argues, "Maruyama clearly does not describe or suggest the use of the memory that includes the security attribute data structure and the selected memory page. However, examiner respectfully disagrees. Maruyama discloses the memory unit 10 includes "all of the component in fig. 4 except for the system bus 15, bus adapter 320, processor 330, 340 and low speed bus 13" (column 5, lines 7-11), it is clear from this passage of Maruyama that the Master ID Table and the DRAM 19 are within and part of the memory unit 10, therefore applicant argument is not persuasive.

Applicant further argues that Maruyama "does not teach that the bus master identification table 24 should be hosted on the DRAM 19 that includes the accessed memory pages" is not persuasive. Applicant acknowledges that DRAM 19 includes the accessed memory pages and Maruyama clearly teaches that the memory unit 10 among the other components includes a DRAM 19 and a Master ID table 24, therefor the memory unit 10 includes the Master ID Table 24 and the selected memory pages which are included in the DRAM 19 (see fig.4 and column 5, lines 7-11).

In response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in

the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988) and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, It would have been obvious to one of ordinary skill in the art at the time the invention was made to integrate the protection features disclosed in applicant's admitted prior art to the memory management system of Maruyama. This would have been obvious because person having ordinary skill in the art at the time the invention was made would have been motivated to do so since these features would add further security to the system by allowing the further access controls such as user or supervisor assigned memory areas and memory areas assigned as read-only or read-write areas.

Applicant's argument that "Maruyama therefor teaches away from using a linear address to access at least one security attribute data structure located in a memory to obtain a security attribute of a selected memory page in the memory" is not persuasive. As it was discussed above Maruyama clearly teaches using a linear address to access at least one security attribute data structure (Master ID Table 24) located in the memory (memory unit 10) to obtain a security attribute of selected memory page in the memory (see fig. 4 and associated text, column 5, lines 7-11 and column 6, lines 29-40).

**(11) Related Proceeding(s) Appendix**

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

Ali S. Abyaneh

A.A

Conferees:

Gilberto Barron

GILBERTO BARRON JR.
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100

Benjamine Lanier